Assignment 1 Signal Integrity

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# Question 1

A graph of a number of waves

Description automatically generated

A graph of a waveform

Description automatically generated

A graph of a square wave

Description automatically generated

A graph with different colored lines

Description automatically generated

The inference to this are fairly simple. The shorter the rise time of a signal, the more harmonics that need to be preserved. It is the high frequency content that allows for sharp edges on signals. As for whether an interconnect is short or long. Take the fundamental frequency and look at some harmonic of that (let’s say the 41st harmonic). Convert that 41st harmonic to wavelength and compare that wavelength with the interconnect length. If the interconnect is less than say the wavelength of that 41st harmonic by ten, the interconnect is electrically short. Otherwise it is electrically long. The “ten” could be any number really and just depends on the tolerable risk in the design/ situation.

# Question 2

HSPICE wasn’t working (don’t have access yet, working on it), So I simulated this in AWR (using method of moments instead of spice). To get at the RLGC parameters, the S parameters were simulated at 1 and 2 GHz, then they were converted in MATLAB using the s2rlgc command. See paper solution for comparisons

A diagram of a computer

Description automatically generated

Figure 1: Schematic

A blue line drawing of a stack of metal

Description automatically generated with medium confidence

Figure 2: Stickup and Substrate Defs

A black line on a white background

Description automatically generated

Figure 3: EM Structure

A grid of squares with black squares

Description automatically generated with medium confidence

Figure 4: EM Structure Mesh

# Question 3

A screenshot of a computer screen

Description automatically generated

A screenshot of a graph

Description automatically generated

A screen shot of a graph

Description automatically generated

The approximation of 0.35 on rise time for the signal bandwidth is a good approximation, but it does not tell the whole story. The bandwidth of the pulse signal is really infinite, however, the amplitudes of the harmonics eventually become insignificant. This happens around the 0.35 on rise time point. To double check this, a clock signal with the correct pulse shape was created. That signal was then transformed to get the spectrum to compare against the theoretical. The first two plots show good agreement, however the third (1ns pulse width) is off by a large factor. I’m still not sure where that came from but it probably has to do with how I’m normalizing the FFT computation. I’m using some tricks to speed up the FFT computation in MATLAB so maybe that is where the shift is coming from

# Question 5

## Part A: Current Issues in Signal and Power Integrity associated with High-Speed Designs

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| --- | --- | --- | --- |
| Issue Number | Issue | Issue Description | Possible Solutions |
| A1 | Cross talk | Electric and Magnetic field coupling between traces that are “close”. ISI also a problem | Better shielding. Going to coplanar waveguides Using differential lines Nothing, crosstalk is basically unavoidable in realistic designs but it can be corrected for using channel estimation techniques and DSP. Also when designing new ICs, add more grounds and power lines so that the return paths are better defined (each pin should be beside a ground or power pin ideally, this is actually being done in FPGA/ ASIC designs now – saw this in a talk on the Altium youtube channel, cant remember which video though). Make sure every layer on a PCB is adjacent to a GND layer this reduces EMI and cross talk issues as the fields will couple less. Also route signals as close to return path as possible |
| A2 | Attenuation | (Usually) undesired power loss/ dissipation in lossy trace | Make the lines shorter but that isn’t always possible Use PIC (Photonics Integrated Circuit) technology/ optical TXRX |
| A3 | Reflections | Signals are really EM waves. Those waves reflect when an impedance boundary is encountered. Ringing, jitter, DCD also a problem | Take trace impedance into consideration. Try to match lines better. Use more reliable substrates with better tolerances (dimensions, dielectric constants). Terminate lines properly in the IC. |
| A4 | EMI/ EMC | Traces/ any EM field with a time derivative not equal to 0 will radiate no matter what. There are laws limiting the radiated power/ energy which restricts which products can go to market. Major offenders are usually the PDN nets/ traces as they usually have the highest current levels. | Design PDN traces to mitigate the EMC problems. Go through the EMC pre-compliance testing in house vs after the fact. Make sure every layer on a PCB is adjacent to a GND layer this reduces EMI and cross talk issues as the fields will couple less. |
| A5 | Delay | EM waves take time to move from one point to another. This is unavoidable since the max speed is the speed of light (but that’s only for free space) | Unavoidable as this is just a reality of EM waves Mitigations could be using different substrates with more favourable dielectric constants. Reduce trace lengths. Design systems to take this into account (such as using the caches instead of RAM and look ahead pipelining) |
| A6 | Noise | Random motion of particles (from thermal, shot, flicker, …) induce unwanted random voltage and current fluctuations. This causes degradation in the SNR. Noise from PDN also a problem (any (voltage) noise added to the signal looks like phase noise on the signal – one of the big results from the PLL class that I took last semester) | Not much can be done about this other then better shielding/ filtering (and good thermal design). Reduce the temp of the system with TEC although that isn’t really done outside of photonics as far as I can tell. Also just simulate for the thermals to make sure there isn’t excessive heat generation/ stagnation |
| A7 | Ground Bounce | A shared return path/ ground path has a voltage across it when there is a switching current. This messes with voltage reference levels | Add more ground pins on ICs (ideally every signal pin is beside a ground or power pin), that way there is less ground bounce on every ground pin since there will be more of them |
| A8 | Signal/ Clock Skew | When traces are different lengths, there will be relative skew. This could be for a clock line or for a differential line | Length match the relevant traces to within some tolerance |

### Highlights from Power and Signal Integrity Simplified (3rd Edition Eric Bogatin)

*Top Ten SI Principles (Page xxvii, paraphrased from preface)*

1. SI matters, take it into account from the beginning. Use analysis tools to accurately predict performance. Use measurement as a way to validate those predictions and reduce risk. The first rule of simulations is they are great, but they are not a substitute for measurements.
2. The separation from screwing around and science/ engineering is putting numbers in. There are 4 important parts of engineering: rules of thumb, analytic approximations, numerical simulations and measurements. All should be applied in SI engineering
3. Every interconnect is a TL with a signal path and a return path. Signal quality is improved when the characteristic impedance is constant along the line.
4. Think return path instead of ground. TLs are really waveguides. The wave/ power exists in the dielectric space. Keep the return path above or below the signal path for good SI/ EMI performance. Also, there are two types of engineers, those who design antennas intentionally, and everyone else.
5. Remember the current through a cap as the voltage changes. Fringe fields can have enough capacitance at the end of a board to provide a low impedance to a fast edge
6. When the number of H field rings (MFLLs) around a conductor changes, there will be a voltage developed on that conductor.
7. Ground bounce is a consequence of this when current is passing though a common ground line/ return path.
8. The BW of a signal is the highest frequency/ harmonic component of that signal that is significant (compared to the same frequency square wave). The BW of a model is the highest frequency that the model can accurately predict. The signal BW always needs to be less than the model BW.
9. Every formula used in SI is either a definition or approximation. Although there are very few exceptions to this. If accuracy is important, an approximation is not good enough.
10. The most expensive outcome is one that delays the time to ship (the product).

## Part B: Industries and Companies Dealing with Signal and Power Integrity Issues

Industries dealing with SI and PI Issues

1. Telecommunications (Ericsson, Nokia, Cienna)
2. IC fabrication/ design (Skyworks, Cisco, Marvell, StarIC)
3. PCB fabrication (JLC PCB, PCB WAY, Rogers Corporation)
4. Satellite communication (Telesat, Telstra, Starlink, SES, Intelsat S.A)
5. Test and Measurement/ Metrology (Keysight, Rhode and Schwartz, Tektronix, LeCroy)
6. CAD Tooling/ Modeling (Altium, Ansys, Keysight, Synopsis, Dassault)

Speaking fairly generally, most companies who care about SI and PI issues are dealing with them in similar ways. The following are some of the ways they are addressing the SI and PI issues:

1. Hiring SI engineers or engineers that have knowledge of SI (see [R5])
2. Investing in numerical simulation tools/ CAD
3. Investing in test engineers to thoroughly validate products over a wide variety of conditions to check for all problems (SI included)
4. Continuous education on SI (say through beTheSignal.com/ Eric Bogatin, conferences or blog posts (see [R6])
5. Invest in the quality of their simulation/ modelling tools. According to one of my supervisors, Rogers has a guy that is devoted to making sure the product attribute calculator they provide for their substrates is very accurate. He does this with a lot of careful and thought out measurements. And keeps a paper trail of them as well. (He does a good job apparently and my advisor is quite fond of him)

## Part C: CAD for Signal and Power Integrity

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| CAD Package Number | CAD Package | Associated Company | Description |
| C1 | HSPICE (PrimeSim) | Synopsys | SPICE based simulator for circuits/ devices that have been validated from the foundry. Extensively used in IC, package, board, backplane and SI simulations [R11] |
| C2 | Synopsys Custom Compiler™ design environment | Synopsys | Great for simulation of analog, digital or mixed signal ICs. Synopsys’s response to cadence [R10] |
| C3 | Altium Designer | Altium | Industry standard for PCB design, has built in trace impedance control and stack up management. Rudimentary SI capabilities from what I can tell [R7] |
| C4 | Altium + HFSS/ SIwave | Altium and Ansys | Altium and Ansys recently partnered to allow for easier simulation of PCBs in high speed designs. [R8] |
| C5 | HFSS | Ansys | Full EM (3D, 2D or 2.5D) simulations of structures. Uses FEA/ FEM [R9] |
| C6 | CST Studio Suite (Simula) | Dassault | “High Performance” 3D EM analysis and simulation software for components/ systems. Good for EMC/ EMI simulations [R12] |
| C7 | Cadence (Sigrity Signal and Power Integrity/ Allegro PCB) | Cadence | Can work with power-aware components/ simulations to model SI/ PI with PCBs and ICs together [R13] |
| C8 | AWR/ Microwave Office | Cadence | EM 3D/ 2D/ 2.5D simulator used to simulate high frequency structures. Also has spice engine built in and can do PCB/ component simulations as well. Used extensively at Ericsson [R14] |
| C9 | PollEx | Altair | Plugin for other programs (currently just Altium). Can simulate for many things (SI, EMI, ESD good diff pairs and return path routing). Looks interesting, I should check this out [R15] |
| C10 | Feko | Altair | Typically used to simulate antennas, can do EMI/ EMC simulations as well. Uses method of moments [R16] |
| C11 | ADS | Keysight | Popular simulation/ design software by keysight. Can also be used for SI purposes [R17] |
| C12 | Synopsys PrimeWave Simulation Environment | Synopsis | Further encapsulates HSPICE/ PrimeSim to add addition features (ERC/DRC, Robustness checker, fault detection) [R18] |
| C13 | SIwave |  | Meant for SI, PI and EMI analysis of PCBs (Full wave/ EM simulations can be used). Can also do electro thermal simulations |

## Part D: IEEE Transaction, Conferences, Books on Signal and Power Integrity

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| Resource Number | Title of Resource | Description |
| D1 | IEEE Transactions on Electromagnetic Compatibility | Publishes significant contributions related to EMC/ EMI (bimonthly, journal) [R20] |
| D2 | IEEE Transactions on Signal and Power Integrity | Same as above but for Signal Integrity topics. Seems new as well (2021) [R21] |
| D3 | IEEE EMC+SIPI Annual Symposia | Conference on SI and PI lasting for 4 days, happens every year [R22] |
| D4 | 2022 IEEE INTERNATIONAL SYMPOSIUM  ON ELECTROMAGNETIC COMPATIBILITY,  SIGNAL & POWER INTEGRITY | Confrence/ education on SI, PI and EMC techniques [R23] |
| D5 | beTheSignal.com | Eric Bogatins Website (offers webinars on SI) [R24] |
| D6 | Signal and Power Integrity Simplified 3rd Edition | Eric Bogatins Book |

## Part E: References

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| Reference Number | Reference |
| [R1] | <https://semiengineering.com/ensuring-signal-and-power-integrity-in-todays-high-speed-designs/> |
| [R2] | <https://resources.pcb.cadence.com/blog/2019-signal-integrity-design-considerations-for-high-speed-design> |
| [R3] | <https://www.keysight.com/blogs/en/tech/sim-des/2018/08/28/5-ways-to-overcome-signal-and-power-integrity-challenges-with-simulation> |
| [R4] | <https://en.wikipedia.org/wiki/List_of_communication_satellite_companies> |
| [R5] | <https://www.linkedin.com/jobs/signal-integrity-engineer-jobs-ottawa-on/?currentJobId=3723351858&originalSubdomain=ca> |
| [R6] | <https://www.keysight.com/blogs/en/tech/sim-des/2018/08/28/5-ways-to-overcome-signal-and-power-integrity-challenges-with-simulation> |
| [R7] | <https://resources.altium.com/p/high-speed-design> |
| [R8] | <https://www.altium.com/documentation/altium-designer/interfacing-with-ansys-simulation-tools> |
| [R9] | <https://www.ansys.com/products/electronics/ansys-hfss> |
| [R10] | <https://www.synopsys.com/implementation-and-signoff/custom-design-platform/custom-compiler.html> |
| [R11] | <https://www.synopsys.com/implementation-and-signoff/ams-simulation/primesim-hspice.html> |
| [R12] | <https://www.3ds.com/products/simulia/cst-studio-suite> |
| [R13] | <https://www.cadence.com/en_US/home/tools/system-analysis/signal-and-power-integrity.html> |
| [R14] | <https://kb.awr.com/display/awrvideos/Signal+Integrity+Modeling+of+High-Speed+Analog+Nets> |
| [R15] | <https://altair.com/pollex-for-ecad> |
| [R16] | <https://altair.com/feko> |
| [R17] | <https://www.keysight.com/us/en/assets/7018-02333/white-papers/5990-4783.pdf> |
| [R18] | <https://www.synopsys.com/implementation-and-signoff/ams-simulation/primewave.html> |
| [R19] | <https://www.ansys.com/products/electronics/ansys-siwave> |
| [R20] | <https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=15> |
| [R21] | <https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=9745882> |
| [R22] | <https://www.emcs.org/virtual-and-webinar-events/ieee-symposia-schedule/> |
| [R23] | <https://emc2022.emcss.org/> |
| [R24] | <https://www.bethesignal.com/bogatin/essential-principles-signal-integrity-p-833.html> |